The MT84SR Recloser of Matis

Communication Protocol

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Catalogue

1 Protocol Specification

This device uses Modbus RTU communication protocol, allowing users to read and write device parameters via Modbus commands. Unless otherwise specified, all values in this protocol are in hexadecimal format.

2 Frame FORMAT SUMMARY

Modbus frame format

Address code	FC	Data field	Check code

2.1 Address Code

- occupies 1 byte;
- Each device terminal corresponds to an address code within the range of 1 to 32 (0x01 to 0x20). The value 0 is a broadcast address, which allows data reading but not configuration.

2.2 FC

- occupies 1 byte;
- According to the definition of the standard Modbus protocol function code, two common basic function codes are selected as the read and write function codes of this protocol.

Function code definition

FC	Act on
0x03	Read hold register
0x06	Write single register

2.3 Data Field

- The format of data field is determined by function code.
- Read register 0x03
- The data field of the response frame consists of the number of bytes and data in the corresponding range of registers.

0x 03 Read Register Frame Format

Request frame			Response frame		
Frame format	Value/Range	Bytes	Frame format	Value/Range	Bytes

Address code	0～247	1	Address code	0～247	1
FC	0x03	1	FC	0x03	1
Resident memory starting address	0 ～ 0xFFFF	2	Return data length	2*N	1
Number of Registrars N	1～125	2	Return data	2～250	2*N
CRC verification		2	CRC verification		2

Note: For frame data containing 2 bytes (except CRC), the high byte is before the low byte.

- Write to single register 0x06

  Write a single hold register, primarily used for parameter configuration, occupying 8 bytes. The return frame matches the request frame. The register value is the written value.

0x 06 Writes a Single Register Frame Format

Request frame			Response frame		
Frame format	Value/Range	Bytes	Frame format	Value/Range	Bytes
Address code	0～247	1	Address code	0～247	1
FC	0x06	1	FC	0x06	1
Residency address	0 ～ 0xFFFF	2	Register address	0～0xFFFF	2
Register value	0 ～ 0xFFFF	2	Register value	0～0xFFFF	2
CRC verification		2	CRC verification		2

2.4 Check Code

The CRC-16 (polynomial A001) is used to generate the check code, with the low byte preceding the high byte.

2.5 MODBUS Abnormal Response Frame

When the device receives the request frame from the master station and successfully processes the data in the request frame, it returns a normal response frame to the master station. If the device fails to receive the request frame from the master station, it does not perform any operation and returns nothing. The master station can set a timeout time as the basis for determining device failure.

When the device receives a request frame from the master station, if the function code or register in the frame fails to meet the data definition requirements,

If the device cannot process the requested frame data, it must return an error response frame to the master station. The format of the error response frame is shown in the table below:

MODBUS Abnormal Response Frame Format

Anomalous response frame		
Frame format	Value/Range	Byte size
Address code	0～247	1
FC	0x80 + Request Function Code	1
Exception code	01/02/03	1
CRC verification		2

The function code is the high bit of the received request frame's function code, indicating that the frame is an abnormal response frame.

The exception code is defined in the following table:

MODBUS Error Code

Exception code	Name	Meaning
01	Illegal function code	The function code of the request frame is not defined
02	Illegitimate register address	The register address of the request frame is not defined
03	Illegitimate register value	The register value or register length in the request frame does not conform to the defined format.

3 Registry DEFINITION

10 radix Address	Data item	Read and write properties	Scale	Windows default	Data type	Byte length	Unit
00	Postal address	R/W	1~247	1	byte	2	
01	Communication baud rate	R/W	1：2400 2：4800 3：9600	1	byte	2	
02	Communication check bit	R/W	1 No check 2 Even 3 : Odd check	2	byte	2	
03	Closing delay compensation	R/W	0~100	30	byte	2	MS
04	Compensation for time delay of circuit breaker	R/W	0~100	5	byte	2	MS
05	Closing reset delay	R/W	0~100	16	byte	2	MS
06	Splitting reset delay	R/W	0~100	16	byte	2	MS
07	Automatic overlap stabilization	R/W	10~600	30	byte	2	S
08	Automatic overlap delay	R/W	1~60	10	byte	2	S
09	Enable auto-replace	R/W	0 ： close 1 ： enable	1	byte	2	
10	Device operation mode	R	1 ： control model 2 ： automatic mode 3 ： manual mode	2	byte	2	
11	Current fault count	R		0	byte	2	

12	Current fault co-unt	R		0	byte	2	
13	Display status	R/W	1 ： red lantern 2 ： green light 3 ： yellow light 4 ： blinking red lamp 5 The green light is flashing. 6 The yellow light is flashing. 7 Red light flash 8 Green light flash 9 Yellow light flash 10 Alternating slow flashes 11 Alternating Flash		byte	2	
14	Lock status	R	0 : Unlocked 1 ： padlock		byte	2	
15	Position Hall Triggered as 1	R	Bit 0: Split Hall Bit 1: Reset Hall Bit 2: Closed Hall				
16	Reclosing state	R	0 ： equipment failure 1 Automatic mode-Open-Trip 2 Automatic mode-Trip-Command 10 : Auto-Close-Man 11 Automatic mode-Close-Command 12 ： automatic mode -		byte	2	

			Close-Auto 20 Manual mode-Open-Manual 30 Manual mode-Close-Manual Decimal data				
17	Control open/ close	W	1 ： separating brake 2 ： switch on 3 ： lock 4 ： deblocking		byte	2	
18	State control	W	2020: System reset	0	byte	2	
19	Chip system voltage	R		0	byte	2	mv
20	OUPA enable	R/W	0 ： close 1 ： enable	1	byte	2	
21	Voltage recovery time	R/W		30	byte	2	S
22	Input power supply voltage	R/W		230	byte	2	V
23	Input power frequency	R/W		50	byte	2	Hz
24	OUPA state	R	0 The voltage is normal. 1 The voltage is normal. 2 The voltage is too high. 3 The voltage is higher than L1:275 V. 4 The voltage is higher than L2: 300V 5 The voltage is higher than L3: 350V 6 Voltage higher		byte	2	

			than				

			L4:400v 7 The voltage is too low. 8 The voltage is lower than L2: 160 V 9 The voltage is lower than L2: 50 V 10 Current fault				
25	High voltage value	R			byte	2	V
26	Low voltage	R			byte	2	V
27	A phase voltage	R			byte	2	V
28	B phase voltage	R			byte	2	V
29	C phase voltage	R			byte	2	V
30	Enable proactive reporting	R/W	0 ： close 1 ： open	1	byte	2	
31	Report status	R		0	byte	2	
32	Software identification number	R			byte	2	S
33	During system operation	R			byte	2	H
34	System operation seconds	R			byte	2	S
35	System count-down	R			byte	2	S
36	Sampling period	R			byte	2	MS
40	Slug UID	R			byte	12	

4 Direction for Use

4.1 Report Proactively

The device will automatically report status changes via RS485 when a status change occurs, with the command format as follows:

Address + Function code (0x07) + Length (1 Byte) + Feedback count (1 Byte) + Feedback status value (1 Byte) + CRC16 (2 Bytes)

Set the interval to 10 seconds for active reporting 3 times. If the corresponding function code (07) is received during this period, the active reporting for this status will stop.

Feedback status value enumeration:

	State	Feedback status value (10-based)	Explain
Automatic mode	485 command to close	1	
	485 command split	2	
	Closing by hand	3	
	Manual disengagement	4	
	Automatic delayed reclosing	5	
	Dry contact control closing	6	
	Dry contact control tripping	7	
	Current fault tripping	8	
	Under-voltage tripping	9	
	Under-voltage recovery closing	10	
	Overvoltage tripping	11	
	Overvoltage recovery closing	12	
	Abnormal disconnection	13	
	Abnormal closing	14	

Example of actively reporting data frames:

Manual disconnection: 01 07 02 00 02 38 B5

Example of actively reporting test feedback data frame (received data):01 07 02 00 02 38 B5

4.2 Communication Control

broadcast instruction

Modbus communication address 0 is a broadcast address. Broadcast addresses can read data but cannot write to the sub-address obtained through broadcast:

[TX] – 00 03 00 00 00 01 85 DB

[RX] – 01 03 02 00 01 79 84

Read address

[TX] -01 03 00 00 00 01 84 0A (default 1, non-default broadcast channel) [RX] -01 03 02 00 01 79 84

Change address

[TX] -01 06 00 00 00 02 08 0B (Change address 1 to 2)

[TX] -02 06 00 00 00 01 48 39 (Change address 2 to 1)

splitting control

[TX] – 01 06 00 11 00 01 18 0F

Compatible instruction [TX] -01 05 00 01 FF 00 DD FA

[RX] – 01 06 00 11 00 01 18 0F

switching control

[TX] – 01 06 00 11 00 02 58 0E

Compatible instruction [TX] -01 05 00 02 FF 00 2D FA

[RX] – 01 06 00 11 00 02 58 0E

Read status

[TX] – 01 03 00 10 00 01 85 CF

[RX] -01 03 02 00 0C B8 41 (Automatic mode-Close-Automatic)Compatible command [TX] -01 03 03 F2 00 01 25 BD

[RX] – 01 03 02 00 02 39 85

The feedback data content matches the status described in this agreement.

5 Version CONTROL

Time	Edition	Event	Handlers
2020/06/10	V1.0	Initial setup	Tang Ji
2020/07/14	V1.1	Modify register definition	Tang Ji
2020/08/18	V1.2	Set register 0x02 as the parity bit	Tang Ji
2020/08/22	V1.3	Register shift	Tang Ji
2020/12/18	V1.4	Add active reporting, unified control, and address reading	Tang Ji
2021/1/29	V1.5	Add active status register 31	Tang Ji
2021/2/22	V1.6	Revise the self-reporting funct-ion description	Tang Ji

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